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(54) **Image scaling apparatus for a multimedia system.**

(57) An apparatus for scaling an image as represented by an arrangement of picture elements. The apparatus scales the image from a first size to a second size based upon plurality of scaling parameters which represent a desired scaling factor. The apparatus includes a scaler circuit which receives the plurality of scaling parameters and an image signal representing the arrangement of picture elements. The scaler circuit manipulates the arrangement of picture elements based upon the plurality of scaling parameters to provide a manipulated arrangement of picture elements. The manipulation includes performing different operations on subsets of the picture elements based upon the plurality of scaling parameters. The operations include a drop operation, which omits a pixel which is received by the scaler circuit, a keep operation, which keeps a pixel which is received by the scaler circuit, a dual operation, which averages two pixels which are received by the scaler circuit, and a quad operation, which averages four pixels which are received by the scaler circuit provides the manipulated arrangement of picture elements as a scaled image.

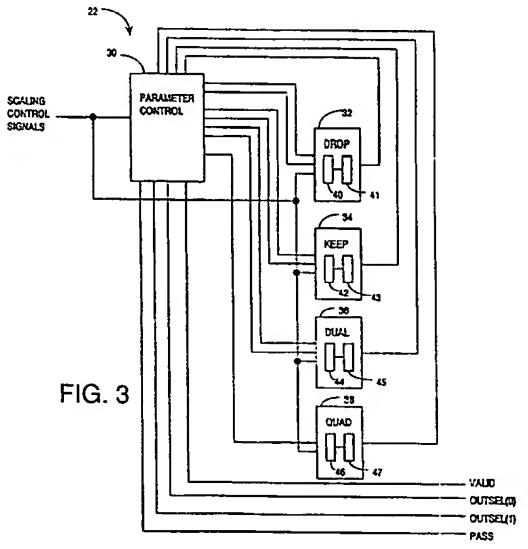

FIG. 3

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The present invention is related to United States Patent Application Serial No. 07/625,564, filed December 11, 1990 of John M. Dinwiddie, Jr., Bobby J. Freeman, Gustavo A. Suarez, and Bruce J. Wilkie, titled "Multimedia System", which application is hereby incorporated by reference.

The present invention relates to multimedia computer systems, and more particularly, to scaling image signals which are used in multimedia computer systems.

Multimedia computer systems are information handling systems which combine the information handling characteristics of traditional computer systems with high quality video and audio presentations. The video presentation is provided by a video display device and the audio presentation is provided by an audio output device.

Multimedia computer systems include media sources which generate media signals. The media signals include audio signals, which are provided to the audio output device, and image signals, which are provided to the video display device. The image signals may include graphics signals, text signals, animation signals and full motion video signals. An image signal is converted to a video presentation by the display device, which receives the image signal and scans the image signal in a raster pattern across a screen of the display device. The speed with which the display device scans the image is called the sweep rate. The screen has a horizontal resolution and a vertical resolution which define display device screen coordinates. Each display device coordinate is a picture element (i.e., a pixel). The presentation from one complete scan of the screen is called a frame, or if the scans are interlaced, the presentation of one complete scan of the screen is called a field. To provide a full motion video presentation, a display device generates multiple frames per second.

By scaling an image it can be represented by an image signal so that the image may be presented on a portion of the screen of the display device (i.e., windower on the screen). Scaling the image allows the image to be simultaneously presented with other images. An example of a system which would use a scaler is the multimedia system which is cross-referenced above.

According to the present invention there is provided an apparatus for scaling an image as represented by an arrangement of picture elements, the apparatus scaling the image from a first size to a second size based upon plurality of variable scaling parameters, the plurality of scaling parameters representing a desired scaling factor, the apparatus comprising a scaler circuit, said scaler circuit being configured to receive the plurality of variable scaling parameters and an image signal representing the arrangement of picture elements, said scaler circuit being configured to manipulate the arrangement of picture elements based upon the plurality of scaling parameters to provide a manipulated arrangement of picture elements, said manipulation including performing different operations on subsets of said picture elements based upon said plurality of scaling parameters, and said scaler circuit being configured to provide said manipulated arrangement of picture elements as a scaled image.

By providing a scaling apparatus which receives an arrangement of picture elements and performs a plurality of operations on the picture elements in response to predefined scaling parameters, an image may be efficiently scaled in real time (i.e., at the image refresh rate) via a low complexity hardware implementation.

Brief Description of the Drawings

Fig. 1 shows a block diagram of a scaling apparatus according to the present invention.

Fig. 2 shows a block diagram of a horizontal component scaling circuit of the Fig. 1 scaling apparatus, the vertical scaling circuit being similar.

Fig. 3 shows a block diagram of the control circuit of the Fig. 2 component scaling circuit.

Fig. 4 shows a block diagram of the signal manipulation circuit of the Fig. 2 component scaling circuit.

Fig. 5 shows a flow chart of the operation of the Fig. 2 scaling apparatus.

Fig. 6 shows a flow chart of the operation of the drop module of the Fig. 2 apparatus.

Fig. 7 shows a flow chart of the operation of the keep module of the Fig. 2 apparatus.

Fig. 8 shows a flow chart of the operation of the dual module of the Fig. 2 apparatus.

Fig. 9 shows a flow chart of the operation of the quad module of the Fig. 2 apparatus.

Fig. 10 shows an alternate embodiment of a scaling apparatus which is in accordance with the present invention.

Detailed Description

Referring to Fig. 1, scaling apparatus 10, which scales a monochromatic image signal (IM), includes scaler control circuit 12 as well as horizontal component scaling circuit 14(h) and vertical component scaling circuit 14(v) (referred to generally as component scaling circuit 14). Scaler control circuit 12 receives control information and provides scaling control signals. The scaling control signals include scaling parameters which are based upon a desired scaling factor; the scaling parameters are generated, e.g., via a look-up table. The control information includes information indicative of the desired scaling factor as well as timing information. Scaler control circuit 12 provides scaling parameters that correspond to the scaling factors to horizontal component scaling circuit

14(h) and vertical component scaling circuit 14(h) as part of the control information. Horizontal scaling circuit 14(h) also receives the IM image signal, which includes an arrangement of pixels of an image to be scaled. The arrangement includes rows and columns of pixels. Horizontal scaling circuit 14(h) manipulates rows of the IM signal by performing a plurality of operations on the IM signal based upon the scaling parameters and provides an intermediate horizontally scaled image signal (HSIM) to vertical component scaling circuit 14(v). Vertical component scaling circuit 14(v) receives the HSIM signal, manipulates columns of pixels in the HSIM signal by performing a plurality of operations on the HSIM signal based upon the scaling parameters and provides a scaled image signal (SIM) which represents a manipulated arrangement of pixels. The manipulated arrangement of pixels correspond to a scaled representation of the IM signal.

Referring to Fig. 2, horizontal component scaling circuit 14(h) includes: input circuit 20, which receives and synchronises the image signal to be scaled as well as clock signals related to the image signal; control circuit 22, which receives the scaling parameters from scaler control circuit 12 and clock signals from input circuit 20 and generates signal manipulation control signals; signal manipulation circuit 24, which manipulates the synchronised image signal based upon signal manipulation control signals which are provided by control circuit 22; and, output circuit 26, which appropriately conditions the scaled image signal to provide the proper format for output. Output circuit 26 of horizontal component scaling circuit 14(h) includes drivers to drive the horizontally scaled image signal to vertical component scaling circuit 14(v).

Vertical component scaling circuit 14(v) is architecturally similar to horizontal component scaling circuit 14(h). However, output circuit 26 of vertical component scaling circuit 14(v) includes a digital to analog converter (not shown) so that the scaled image signal is in the proper format for display.

Referring to Fig. 3, control circuit 22 includes parameter control circuit 30, which receives a plurality of scaling control signals from scaler control circuit 12 as input control signals. These input control signals include a pixel clock signal (PIXEL CLK), a load register signal (IOW), an enable signal (F), which enables a rear or write signal based upon a decode of the load address, two address select bits (A0 and A1), which represent the least significant bits of the load address, and a blanking signal (BLNK), which is a timing signal which indicates when the display device is in its retrace interval. Control circuit 22 also includes drop circuit 32, keep circuit 34, dual circuit 36 and quad circuit 38, which receive a drop control signal (DROP), a keep control signal (KEEP), a dual control signal (DUAL) and a quad control signal (QUAD), respectively, as well as the PIXEL CLK signal from control circuit 12. The DROP, KEEP, DUAL, and QUAD signals are the scaling parameters which are provided by scaler control circuit 12. Drop circuit 32 includes drop register 40 and drop counter 41. Keep circuit 34 includes keep register 42 and keep counter 43. Dual circuit 36 includes dual register 44 and dual counter 45. Quad circuit 38 includes quad register 46 and quad counter 47. Each register 40, 42, 44, 46 is a conventional 8-bit register. Each counter 41, 43, 45, 47 is a conventional loadable 8-bit down counter.

Drop circuit 32 provides an 8-bit drop count signal (DROP CNT) as well as a drop feedback signal (DROPZ), which indicates when the DROP CNT signal equals zero, as input control signals to parameter control circuit 30. Keep circuit 34 provides an 8-bit keep count signal (KEEP CNT) as well as a keep feedback control signal (KEEPZ), which indicates when the KEEP CNT signal equals zero, as input control signals to parameter control circuit 30. Dual circuit 36 provides an 8-bit dual count signal (DUAL CNT) as well as a dual feedback control signal (DUALZ), which indicates when the DUAL CNT signal equals zero, as input control signals to parameter control circuit 30. Quad circuit 38 provides a quad feedback control signal (QUADZ), which indicates when the count which is provided by the counter portion of quad circuit 38 equals zero, as input control signals to parameter control circuit 30.

Parameter control circuit 30 provides a plurality of output signals including a counter initialisation signal (INITCTR), which is provided to the counters 41, 43, 45, 47 of drop circuit 32, keep circuit 34, dual circuit 36 and quad circuit 38. Other output signals provided by parameter control circuit 30 include a load drop register signal (LDDR) and a decrement drop counter signal (DECDC), which are provided to drop circuit 32, a load keep register signal (LDKR) and a decrement keep counter signal (DECKC), which are provided to keep circuit 32, a load dual register (LDDAR) and a decrement dual counter signal (DECDAC), which are provided to dual circuit 34, and a load quad register (LDQAR) and a decrement quad counter signal (DECQAC), which are provided to quad circuit 36. Parameter control circuit 30 also provides a plurality of signal manipulation output control signals including a pass indication signal (PASS), which indicates when to allow a pixel to flow through signal manipulation circuit 24, a 2-bit out select signal (OUTSEL), which controls manipulation of a signal by signal manipulation circuit 24, and a valid output pixel signal (VALID), which indicates when the next stage to which the scaled image signal is provided may read the scaled image signal.

Parameter control circuit 30 includes a plurality of programmable array logic integrated circuits (PALs) which provide the output signals based upon the input signals. The PALs are programmed with PAL equations; each PAL equation corresponds to circuitry

which generates a particular output signal. For PAL equations, a "/" indicates an inversion, a "=" indicates an asynchronous equals, and a ":=" indicates a signal which is synchronised by a flip flop which is clocked by the PIXEL CLK signal. More specifically, the PAL equation for the INITCTR signal is:

INITCNT = (BLNK AND /A AND /B) OR (DROP1 AND KEEPZ AND DUALZ AND QUADZ AND /A AND /B) OR (DROPZ AND KEEP1 AND DUALZ AND QUADZ AND /A AND /B) OR (DROPZ AND KEEPZ AND DUALZ AND QUADZ AND /A AND /B) OR (DUAL1 AND QUADZ AND /A AND B) OR (QUADZ AND A AND /B):

where,

DROP1 = /DROP CNT(7) AND /DROP CNT(6) AND /DROP CNT(5) AND /DROP CNT(4) AND /DROP CNT(3) AND /DROP CNT(2) AND /DROP CNT(1) AND DROP CNT(0);

KEEP1 = /KEEP CNT(7) AND /KEEP CNT(6) AND /KEEP CNT(5) AND /KEEP CNT(4) AND /KEEP CNT(3) AND /KEEP CNT(2) AND /KEEP CNT(1) AND KEEP CNT(0);

DUAL1 = /DUAL CNT(7) AND /DUAL CNT(6) AND /DUAL CNT(5) AND /DUAL CNT(4) AND /DUAL CNT(3) AND /DUAL CNT(2) AND /DUAL CNT(1) AND DUAL CNT(0);

A := B AND DUALZ AND /QUADZ;

and,

B := (DUALZ AND /QUADZ AND /A AND B) OR (/BLNK AND DROPZ AND KEEPZ AND /DUALZ AND /A AND /B) OR (/BLNK AND DROPZ AND KEEPZ AND /QUADZ AND /A AND /B).

The PAL equation for the LDDR signal is:

LDDR = IOW AND F AND A1 AND A0.

The PAL equation for the DECDC signal is:

DECDC = /BLNK AND /DROPZ AND /A AND /B,

where A and B are refined above. The PAL equation for the LDKR signal is:

LDKR = IOW AND F AND A1 AND /A0.

The PAL equation for the DECKC signal is:

DECKC = /BLNK AND /KEEPZ AND DROPZ AND /A AND /B,

where A and B are described above. The PAL equation for the LDDAR signal is:

LDDAR = IOW AND F AND /A1 AND A0.

The PAL equation for the DECDAC signal is:

DECDAC = /A AND B AND /DUALZ,

where A and B are described above. The PAL equation for the LDQAR signal is:

LDQAR = IOW AND F AND /A1 AND /A0.

The PAL equation for the DECDAC signal is:

DECQAC = A AND B,

where A and B are described above.

PALs also control generating the signal manipulation control signals. Accordingly, the PAL equation for the PASS signal is:

PASS = A AND B.

The PAL equation for the OUTSEL(1) signal is:

OUTSEL(1) = A AND /B.

The PAL equation for the 0UTSEL(2) signal is:

OUTSEL(2) = /A AND B AND /DUALZ.

The PAL equation for the VALID signal is:

VALID := A AND /B OR /DUALZ AND /A AND /B OR /BLNK AND DROPZ AND /KEEPZ AND /A AND /B.

Control circuit 22 works in conjunction with signal manipulation circuit 24 based upon the states of the signal manipulation control signals and the clock signals.

Referring to Fig. 4, signal manipulation circuit 24 includes: adder circuit 50, which receives the synchronised IM signal; shifter circuit 52, which receives an output from adder circuit 50 as well the OUTSEL control signal from parameter control circuit 30 of control circuit 22; register circuit 54, which receives the output signal from shifter circuit 52 as well as the PIXEL CLK clock signal; and, zeroing circuit 56, which receives the synchronised output signal from register circuit 54 as well as the PASS control signal. Zeroing circuit 56 provides a second input to adder circuit 50.

Referring to Fig. 1, in operation, scaler control circuit 12 receives control information which indicates the desired ratio by which an image should be scaled (i.e., a scaling factor). Scaler control circuit 12 provides four scaling parameters, a drop parameter, a keep parameter, a dual parameter and a quad parameter, to component scaling circuits 14(h) and 14(v) based upon the scaling factor desired. For example, if the reduction desired is 3/4 of the original image, the scaling parameters are DROP = 0, KEEP = 2, DUAL = 1 and QUAD = 0. If the reduction desired is 1/5 of the original image, the scaling parameters are DROP = 1, KEEP = 0, DUAL = 0 and QUAD = 1. If the reduction desired is 2/3 of the original image, the scaling parameters are DROP = 0, KEEP = 1, DUAL = 1, and QUAD = 0. Component scaling circuits 14 also receive the IM signal, which represents an arrangement of pixels of an image, on a pixel by pixel basis. Horizontal component scaling circuit 14(h) receives the IM signal, horizontally scales this signal, and provides the horizontally scaled image signal HIM to vertical component scaling circuit 14(v). Vertical component scaling circuit 14(v) receives the horizontally scaled image signal and vertically scales this signal to provide the scaled image signal SIM, which represents a manipulated arrangement of pixels.

Each component scaling circuit 14 scales along an axis of the arrangement of pixels by performing a combination of four operations on the pixels of that axis; horizontal component scaling circuit 14(h) scales the abscissa and vertical component scaling circuit scales the ordinate. The operations include a drop operation, a keep operation, a dual operation and a quad operation. With a drop operation, compo-

nent scaling circuit 14 omits a pixel which is received by component scaling circuit 14. With a keep operation, component scaling circuit 14 keeps a pixel which is received by component scaling circuit 14. With a dual operation, component scaling circuit 14 averages two pixels which are received by component scaling circuit 14. With a quad operation, component scaling circuit 14 averages four pixels which are received by component scaling circuit 14. Combinations of these four operations can represent any reduction.The frequency with which the operations are performed corresponds to the four scaling parameters.

More specifically, referring to Figs. 1 and 5, when scaling the horizontal axis of the image, horizontal component scaling circuit 14(h) is activated by scaler control circuit 12. Registers 40, 42, 44, 46 are loaded with the drop, keep, dual and quad parameters, respectively, as set initial parameters block 79. More specifically, the drop parameter is loaded into register 40 as the DROP COUNT signal when the LDDR signal is active. The keep parameter is loaded into register 42 as the KEEP COUNT signal when the LDKR signal is active. The dual parameter is loaded into register 44 as the DUAL COUNT signal when the LDDAR signal is active. The quad parameter is loaded into register 46 as the QUAD COUNT signal when the LDQAR signal is active. Control is then passed to blanking signal review block 80.

When the BLNK signal becomes inactive, as determined by blanking signal review block 80, control is passed to load parameters block 82. In load parameters block 82, the drop, keep, dual, and quad parameters are loaded into counters 41, 43, 45, 47, respectively. When an active INITCNT signal is provided by control circuit 22. Once the scaling parameters are loaded into the counters, component scaling circuit 14(h) is ready to begin scaling the image. If the BLNK signal is active, indicating that the display device scan is inactive, then component scaling circuit 14(h) goes into a wait state, i.e., loops, until the BLNK signal becomes inactive.

After counters 41, 43, 45, 47 are loaded, control is passed to drop module 84. From drop module 84, control is either passed to keep module 86 or is returned to blanking signal review block 80. From keep module 86, control is either passed to dual module 88 or is returned to blanking signal review block 80. From dual module 88, control is either passed to quad module 90 or is returned to blanking signal review block 80. From quad module 90, control is returned to blanking signal review block 80.

More specifically, referring to Figs. 3 and 6, when control is passed to drop module 84, drop module 84 first determines, at drop count decision block 100, whether DROP COUNT is equal to zero. If DROP COUNT is equal to zero, indicating that a drop pixel operation should not occur, then control is passed to keep module 86.

If DROP COUNT is not equal to zero, indicating that a drop pixel operation should occur, then control is passed to perform drop operation block 102. At perform drop operation block 102, parameter control circuit 30 provides an active DECDC signal to counter 41, thus causing counter 41 to decrement the DROP COUNT signal, parameter control circuit 30 sets the VALID signal inactive and the pixel counter is set to the next pixel of the IM signal. When an inactive VALID signal is provided by control circuit 22, the pixel is effectively dropped because the pixel is not read by the next stage before the next pixel is provided to component scaler circuit 14. Signal manipulation circuit 24 does not perform an operation on the pixel when a pixel is dropped.

Perform drop operation block 102 passes control to blanking review block 104, which determines whether the BLNK signal is active. If the BLNK signal is active, control leaves drop module 84 and is returned to blanking signal review block 80. If the BLNK signal is inactive, then control is passed to drop count decision block 100. If the DROP COUNT signal now equals zero, then control is passed to keep module 86, otherwise control is passed to perform drop operation block 102.

Referring to Figs. 3, 4 and 7, when control is passed to keep module 86, keep module 86 first determines, at keep count decision block 110, whether KEEP COUNT is equal to zero. If KEEP COUNT is equal to zero, indicating that a keep operation should not be performed, then control is passed to dual module 88.

If KEEP COUNT is not equal to zero, indicating that a keep pixel operation should occur, then control is passed to perform keep operation block 112. At perform keep operation block 112, parameter control circuit 30 provides an active DECKC signal to counter 43, thus causing counter 43 to decrement the KEEP COUNT signal and parameter control circuit 30 to set the PASS signal active and the VALID signal active.

When an active VALID signal is provided by output circuit 26 in conjunction with an active PASS signal, the pixel is effectively kept because the pixel is read by the next stage before the next pixel is provided to component scaler circuit 14.

In signal manipulation circuit 24 when a pixel is kept, the pixel which is provided to adder circuit 50 as the first adder input signal is added to zero, which is provided by zero circuit 56 as the second adder input signal when the PASS signal is active. The output signal of adder circuit 50 is provided to register circuit 54 where it is provided as an output when the VALID signal becomes active.

Control is passed from keep operation block 112 to blanking review block 114, which determines whether the BLNK signal is active. If the BLNK signal is active, control is returned to blanking signal review

block 80. If the BLNK signal is inactive, control is passed to keep count decision block 110. If the KEEP COUNT signal now equals zero, then control is passed to dual module 88, otherwise control is passed to perform keep operation block 112.

Referring to Fig. 8, when control is passed to dual module 88, dual module 88 first determines, at dual count decision block 120, whether the DUAL COUNT signal is equal to zero. If the DUAL COUNT signal equals zero, indicating that a dual operation should not be performed then control is passed to quad module 90.

If the DUAL COUNT signal does not equal zero, indicating that a dual pixel operation should occur, then control is passed to perform shift right block 122. At shift right block 122, two consecutive input pixels are adder and the sum is shifted right, thus averaging the two pixels. Shift right block 122 then passes control to keep advance block 124. In keep advance block 124, parameter control circuit 30 provides an active DECDAC signal, thus decrementing the DUAL COUNT signal, and sets the VALID signal active. When an active VALID signal is provided by output circuit 26, the averaged pixel is read by the next stage.

Signal manipulation circuit 24 manipulates the input pixels when the shift right portion of the dual operation is performed. More specifically, a first pixel is provided to adder circuit 50, passed through adder circuit 50 and shifter circuit 52 and is stored in register circuit 54. A second consecutive pixel is provided to adder circuit 50. Because the PASS signal is inactive, the first pixel, which is stored in register circuit 54, is passed through zero circuit 56 and provided to adder circuit 50 as the second adder input signal. Adder circuit 50 adds the two pixels and provides the sum to shifter circuit 52. Based upon the state of the OUTSEL signal, shifter circuit shifts the sum right one bit, thus effectively dividing by two. However, any remainder from the shift is discarded.

Dual advance block 124 passes control to blanking review block 126, which determines whether the BLNK signal is active. If the BLNK signal is active, control is returned to blanking signal review block 80. If the BLNK signal is inactive, control is passed to dual count decision block 120. If the DUAL COUNT signal now equals zero, then control is passed to quad module 90, otherwise, control is passed to perform shift right block 122.

Referring to Figs. 3, 4 and 9, when control is passed to quad module 90, quad module 90 first determines, at quad count decision block 130, whether the QUAD COUNT signal equals zero. If the QUAD COUNT signal equals zero, indicating that a quad operation should not be performed, then control is passed to blanking signal review block 80.

If the QUAD COUNT signal roes not equal zero, indicating that a quad pixel operation should be performed, then control is passed to perform shift right two block 132. At shift right two block 132, four consecutive input pixels are added and the sum is shifted right two bits, thus averaging the four pixels. Shift right two block 132 then passes control to quad advance block 134. In quad advance block 134, parameter control circuit 30 provides an active DECQAC signal, thus decrementing the QUAD COUNT signal, and sets the VALID signal active. When an active VALID signal is provided by output circuit 26, the averaged pixel is rear by the next stage.

Signal manipulation circuit 24 manipulates the input pixels during the shift right two portion of the quad operation. More specifically, a first pixel is provided to adder circuit 50, passed through adder circuit 50 and shifter circuit 52 and is stored in register circuit 54. A second consecutive pixel is provided to adder circuit 50. Because the PASS signal is inactive, the first pixel, which is stored in register circuit 54, is passed through zero circuit 56 and provided to adder circuit 50 as the second adder input signal. Adder circuit 50 adds the two pixels and provides the sum to shifter circuit 52. Based upon the state of the OUTSEL signal, shifter circuit passes the sum to register circuit 54. Because the PASS signal is inactive, the sum of the first two pixels, which is stored in register circuit 54, is passed through zero circuit 56 and provided to adder circuit 50 as the second adder input signal. Adder circuit 50 adds the sum of the first two pixels with the third pixel and provides the sum to shifter circuit 52. Based upon the state of the OUTSEL signal, shifter circuit passes the sum to register circuit 54. Because the PASS signal is inactive, the sum of the first three pixels, which is stored in register circuit 54, is passed through zero circuit 56 and provider to adder circuit 50 as the second adder input signal. Adder circuit 50 adds the sum of the first three pixels with the forth pixel and provides the sum to shifter circuit 52. Based upon the state of the OUTSEL signal, shifter circuit shifts the sum of the four pixels to the right two bits, thus effectively dividing the sum of the four pixels by four, and averaging the four pixels. The result of this operation is stored in register circuit 54, from where this result is read when the VALID signal goes active. However, any remainder from the shift is discarded.

Quad advance block 124 passes control to blanking review block 126, which determines whether the BLNK signal is active. If the BLNK signal is active, control is returned to blanking signal review block 80. If the BLNK signal is inactive, control is passed to quad count decision block 120. If the QUAD COUNT signal now equals zero, then control is passed to blanking signal review block 80, otherwise control is passed to perform shift right block 122.

When control is passed to blanking signal review block 80, if the BLNK signal is still inactive, then control is passed to load parameters block 82. When the BLNK signal goes active, indicating that a horizontal

scan line has been completed, then horizontal component scaling circuit 14(h) goes into a wait state until the BLNK signal again becomes inactive, indicating that the next line in the arrangement of pixels is being presented to horizontal component scaler circuit 14(h).

Referring again to Fig. 1, horizontal component scaling circuit 14(h) provides the horizontally scaled image, as represented by the HSIM signal, to vertical component scaling circuit 14(v), which vertically scales the image simultaneously with the horizontal scaling. More specifically, input circuit 20 of vertical component scaling circuit 14(v) receives the HSIM signal from horizontal component scaling circuit 14(h). Input circuit 20 of vertical component scaling circuit 14(v) stores the HSIM signal as lines of pixels which correspond to lines of the presentation. When enough lines have been stored to manipulate pixels along the ordinate, then signal manipulation circuit 24 and control circuit 22 manipulate the pixels. The manipulated pixels are provided to output circuit 26 of vertical component scaling circuit 14(v), where the manipulated pixels are assembled in a memory to provide a frame of the scaled presentation. When the frame is fully assembled as indicated by a vertical blanking signal, then the scaled output signal SIM is provided to a display device where the scaled image is presented.

OTHER EMBODIMENTS

Other embodiments are within the following claims.

For example, Fig. 10 shows an alternate scaler circuit which may be used to scale colour images.

Also, for example, while a hardware implementation is set forth as the preferred embodiment of a scaler according the present invention, a scaler according to the present invention can be implemented using a computer program.

Claims

1. An apparatus for scaling an image as represented by an arrangement of picture elements, the apparatus scaling the image from a first size to a second size based upon plurality of variable scaling parameters, the plurality of scaling parameters representing a desired scaling factor, the apparatus comprising

   a scaler circuit

   said scaler circuit being configured to receive the plurality of variable scaling parameters and an image signal representing the arrangement of picture elements,

   said scaler circuit being configured to manipulate the arrangement of picture elements based upon the plurality of scaling parameters to provide a manipulated arrangement of picture elements,

   said manipulation including performing different operations on subsets of said picture elements based upon said plurality of scaling parameters, and

   said scaler circuit being configured to provide said manipulated arrangement of picture elements as a scaled image.

2. The apparatus of claim 1 wherein said scaler circuit includes a control circuit,

   said control circuit being configured to receive said plurality of scaling parameters and to provide signal manipulation control signals based upon said plurality of scaling parameters, and

   a signal manipulation circuit,

   said signal manipulation circuit being configured to manipulate said arrangement of picture elements in response to said signal manipulation control signals.

3. The apparatus of claim 2 wherein said control circuit includes a parameter counter circuit

   said parameter counter circuit being configured to receive a scaling parameter and to provide a parameter count signal and a parameter count equals zero control signal to said parameter control signal, and

   a parameter control circuit,

   said parameter control circuit being configured to receive input control signals including said parameter count signal and said parameter count equals zero control signal from said parameter counter circuit as well as a timing control signal and a scaling enable signal, to provide said signal manipulation control signals based upon said input control signals and to provide said timing control signal to said parameter counter circuit.

4. The apparatus of claim 3 wherein said control circuit includes a plurality of parameter counter circuits,

   said plurality of parameter counter circuits providing a plurality of parameter count signals and a plurality of parameter count equals zero signals to said parameter control circuit based upon said plurality of scaling parameters and said timing control signal, and

   said parameter control circuit is configured to receive said plurality of parameter count signals and said plurality of parameter count equals zero signals as input control signals.

5. The apparatus of claim 4 wherein said parameter counter circuit is a drop circuit,

   said drop circuit being configured to

receive a drop scaling parameter and to provide a drop count signal as well as a drop count equals zero control signal to said parameter control circuit.

6. The apparatus of claim 4 wherein said parameter counter circuit is a keep circuit,

said keep circuit being configured to receive a keep scaling parameter and to provide a keep count signal as well as a keep count equals zero control signal to said parameter control circuit.

7. The apparatus of claim 4 wherein said parameter counter circuit is a dual circuit,

said dual circuit being configured to receive a dual scaling parameter and to provide a dual count signal as well as a dual count equals zero control signal to said parameter control circuit.

8. The apparatus of claim 4 wherein said parameter counter circuit is a quad circuit,

said quad circuit being configured to receive a quad scaling parameter and to provide a quad count signal as well as a quad count equals zero control signal to said parameter control circuit.

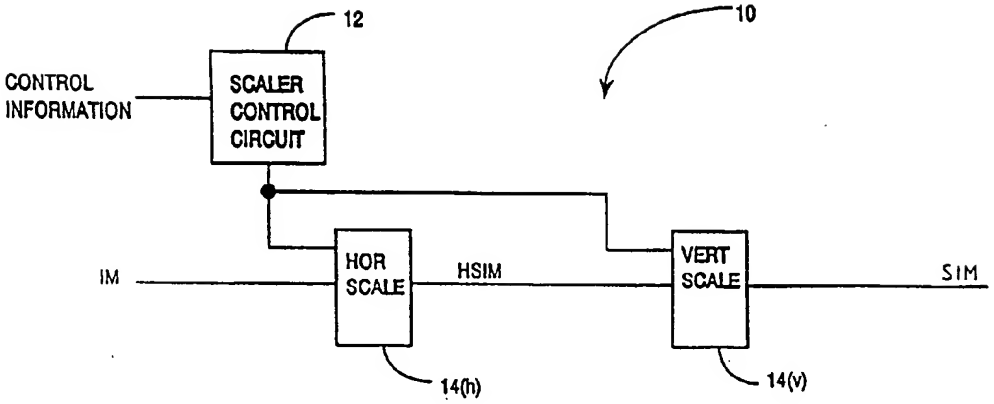
12
10
CONTROL INFORMATION
SCALER CONTROL CIRCUIT
IM
HOR SCALE
HSIM
VERT SCALE
SIM
14(h)
14(v)

FIG. 1

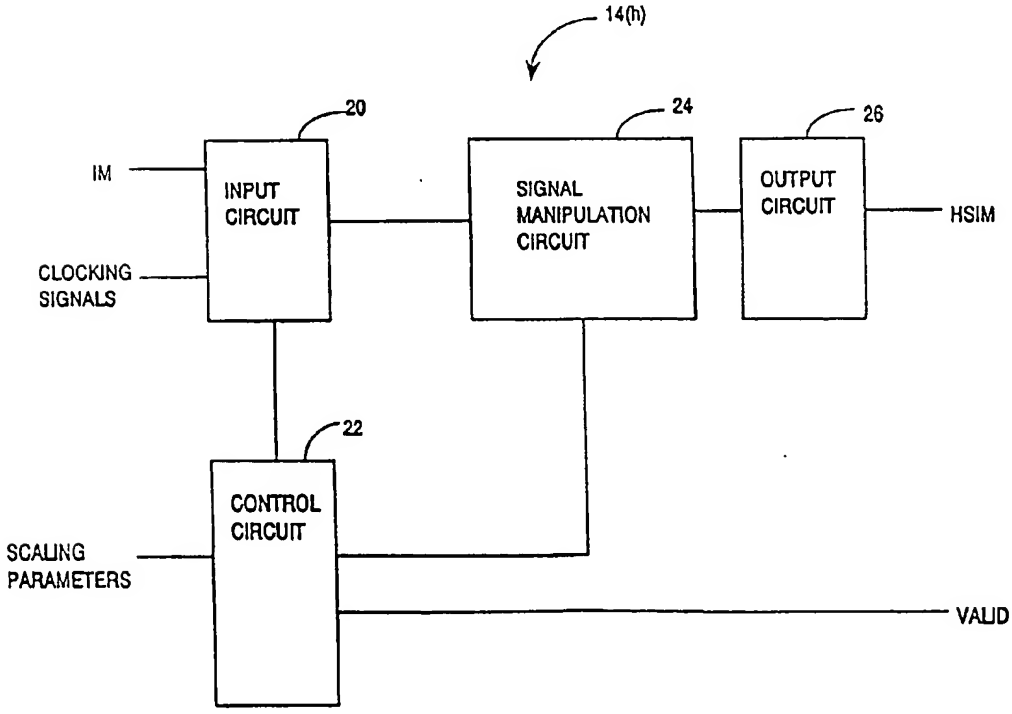
14(h)
20
24
26
IM
INPUT CIRCUIT
SIGNAL MANIPULATION CIRCUIT
OUTPUT CIRCUIT
HSIM
CLOCKING SIGNALS
22
CONTROL CIRCUIT
SCALING PARAMETERS
VALID

FIG. 2

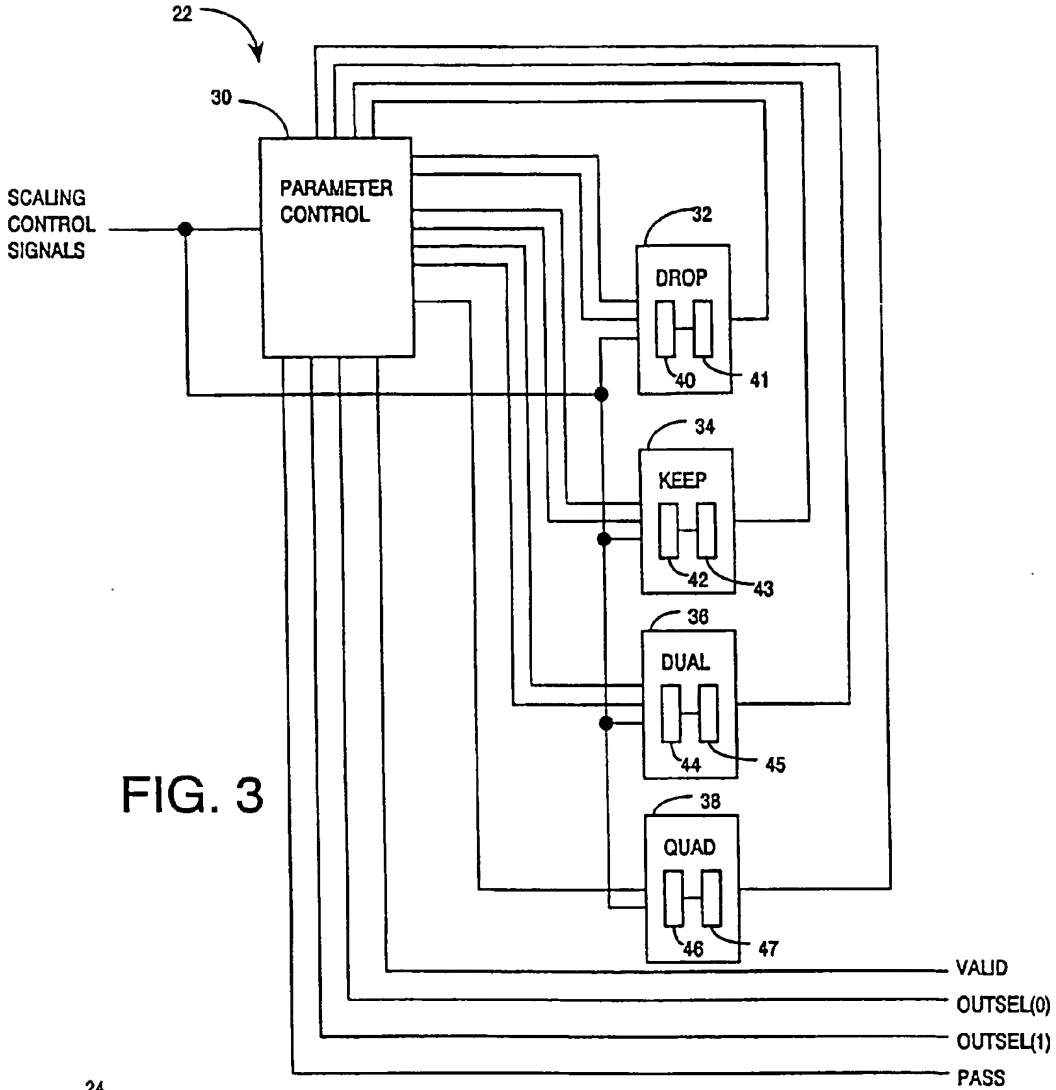
22
30
PARAMETER CONTROL
SCALING CONTROL SIGNALS
32
DROP
40
41
34
KEEP
42
43
36
DUAL
44
45
38
QUAD
46
47
VALID
OUTSEL(0)
OUTSEL(1)
PASS

FIG. 3

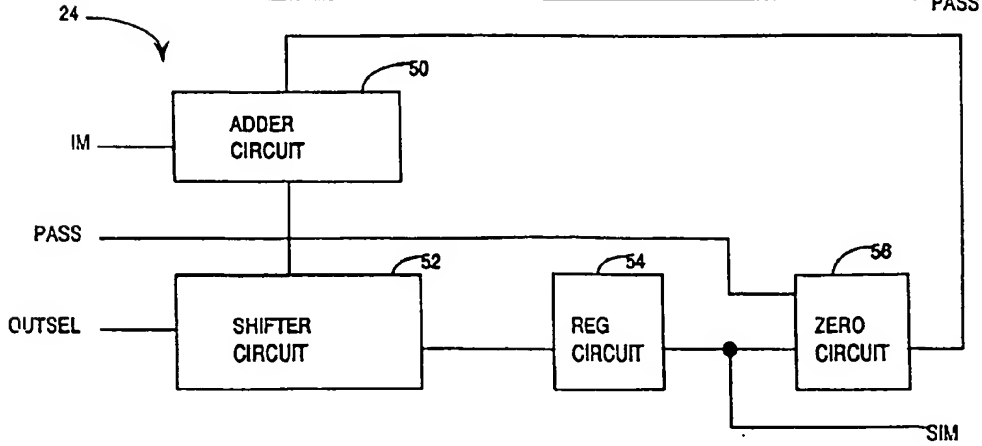
24
50
ADDER CIRCUIT
IM
PASS
52
SHIFTER CIRCUIT
OUTSEL
54
REG CIRCUIT
58
ZERO CIRCUIT
SIM

FIG. 4

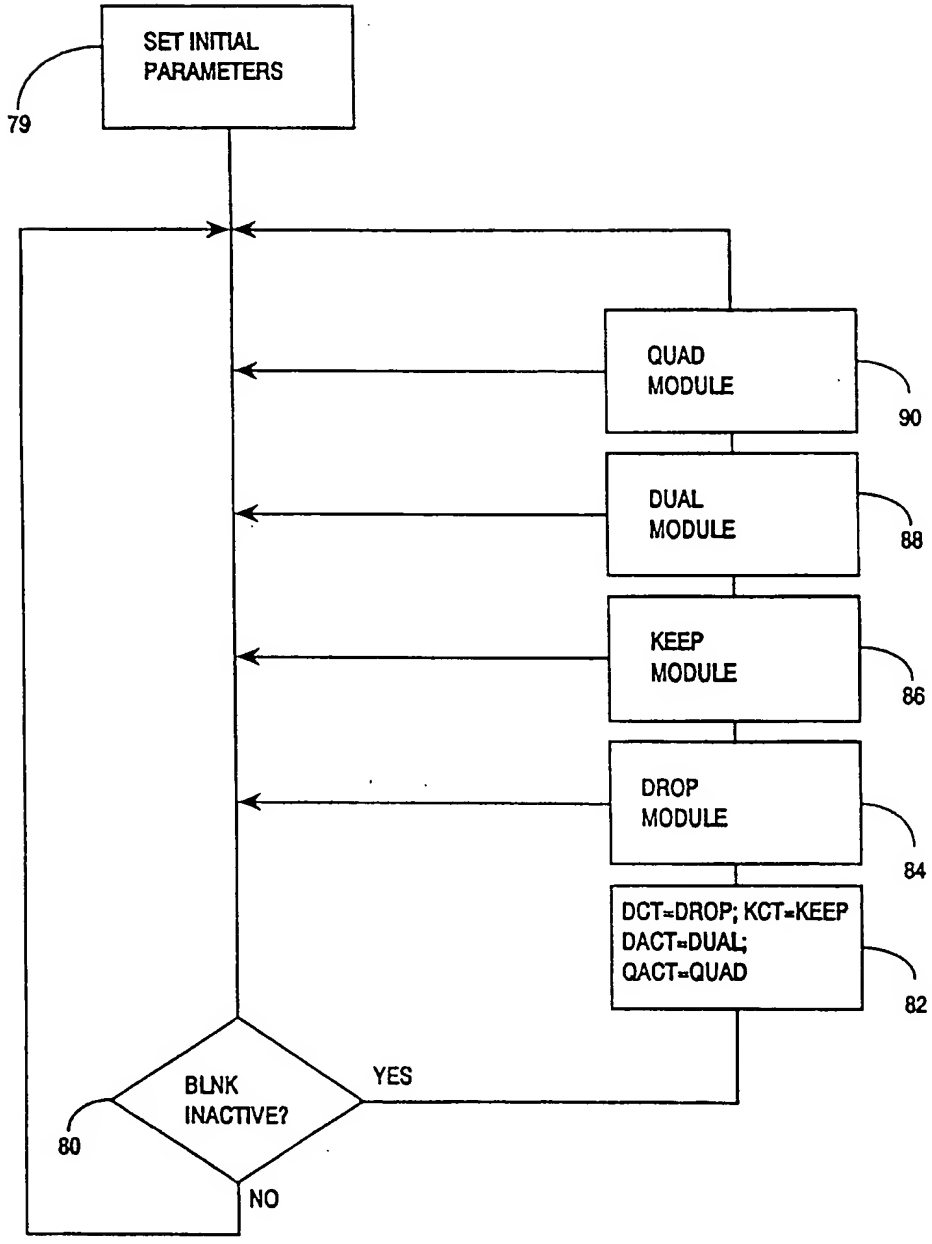
SET INITIAL PARAMETERS
79
QUAD MODULE
90
DUAL MODULE
88
KEEP MODULE
86
DROP MODULE
84
DCT=DROP; KCT=KEEP
DACT=DUAL;
QACT=QUAD
82
BLNK INACTIVE?
80
YES
NO

FIG. 5

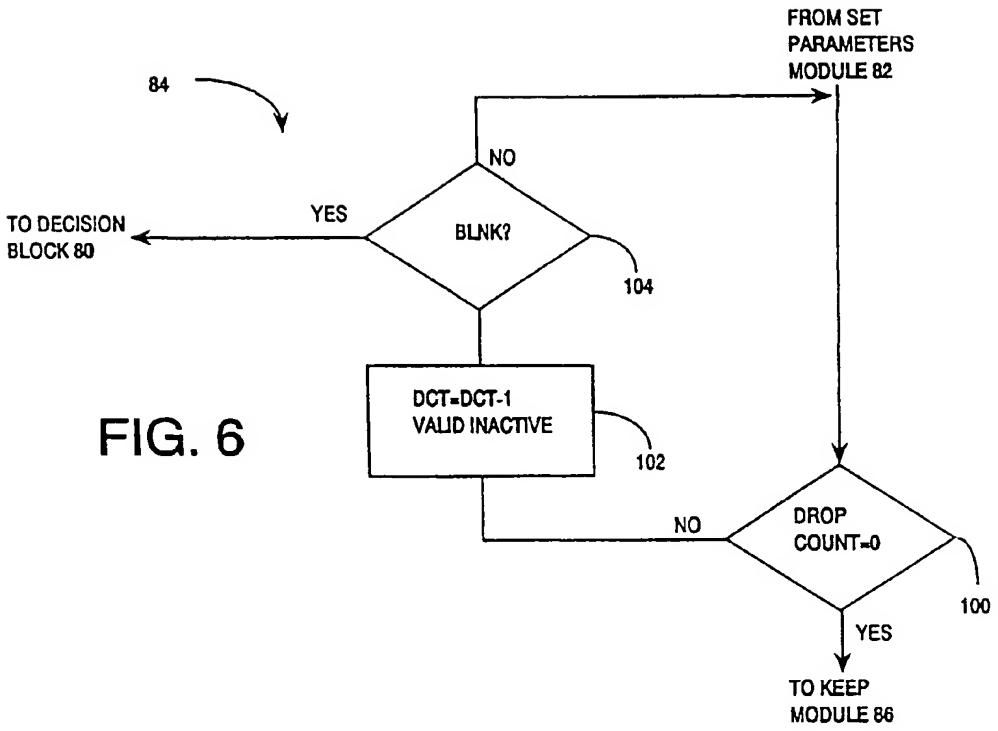
FROM SET
PARAMETERS
MODULE 82
84
NO
YES
TO DECISION
BLOCK 80
BLNK?
104
DCT=DCT-1
VALID INACTIVE
102
NO
DROP
COUNT=0
100
YES
TO KEEP
MODULE 86

FIG. 6

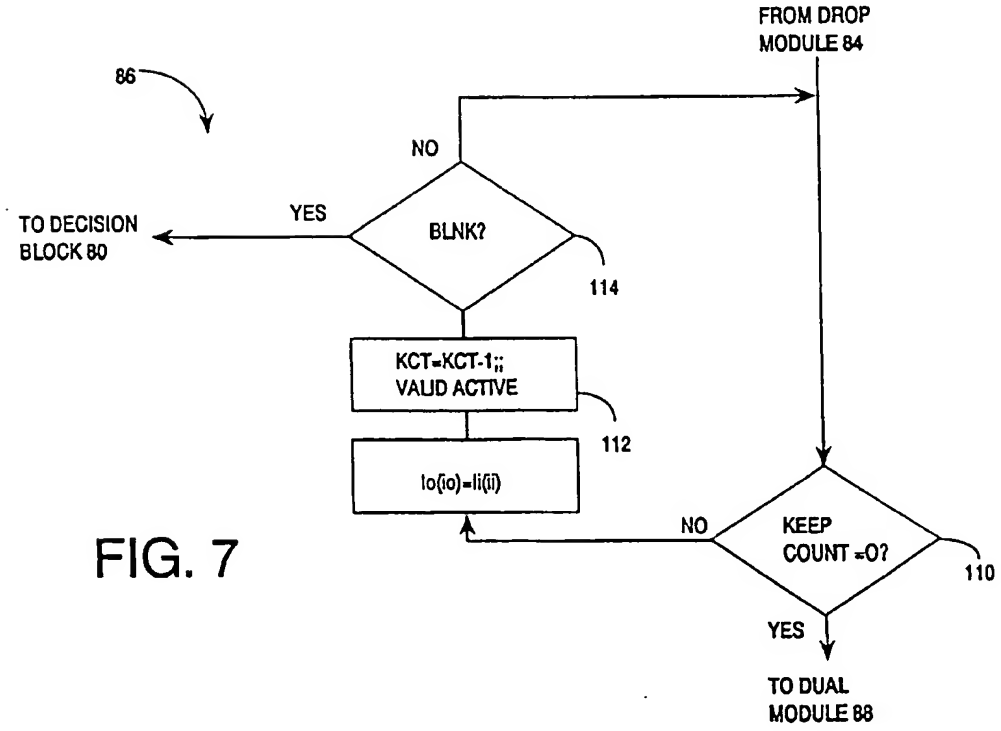
FROM DROP
MODULE 84
86
NO
YES
TO DECISION
BLOCK 80
BLNK?
114
KCT=KCT-1;;
VALID ACTIVE
112
Io(io)=Ii(ii)
NO
KEEP
COUNT =0?
110
YES
TO DUAL
MODULE 88

FIG. 7

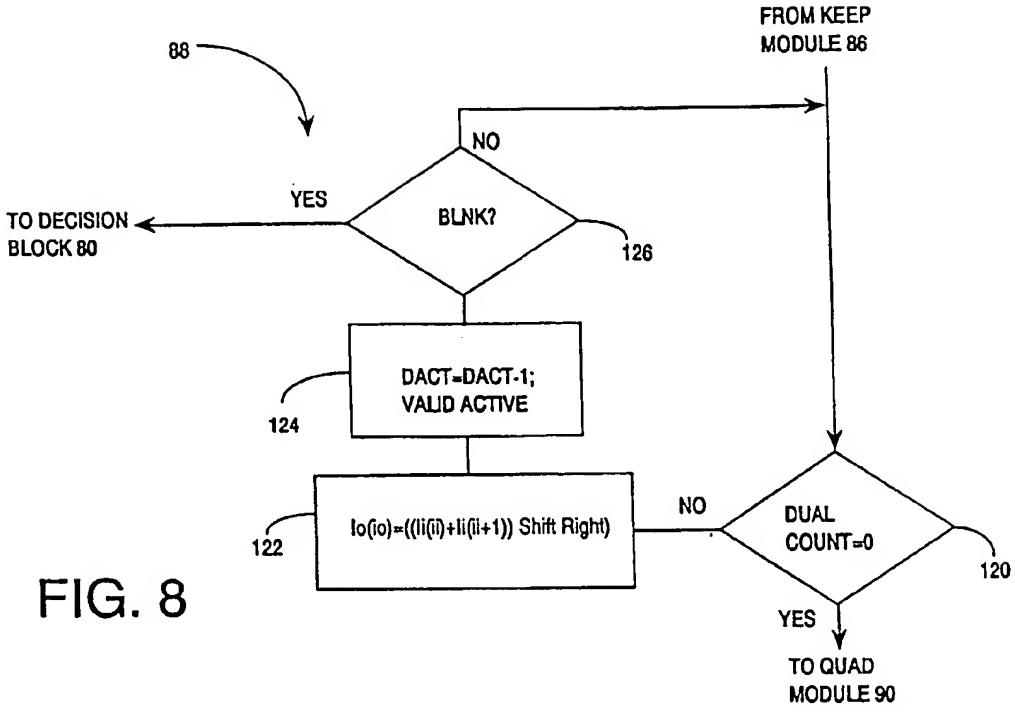
88
FROM KEEP MODULE 86
NO
YES
BLNK?
126
TO DECISION BLOCK 80
DACT=DACT-1; VALID ACTIVE
124
Io(io)=((Ii(ii)+Ii(ii+1)) Shift Right)
122
NO
DUAL COUNT=0
120
YES
TO QUAD MODULE 90

FIG. 8

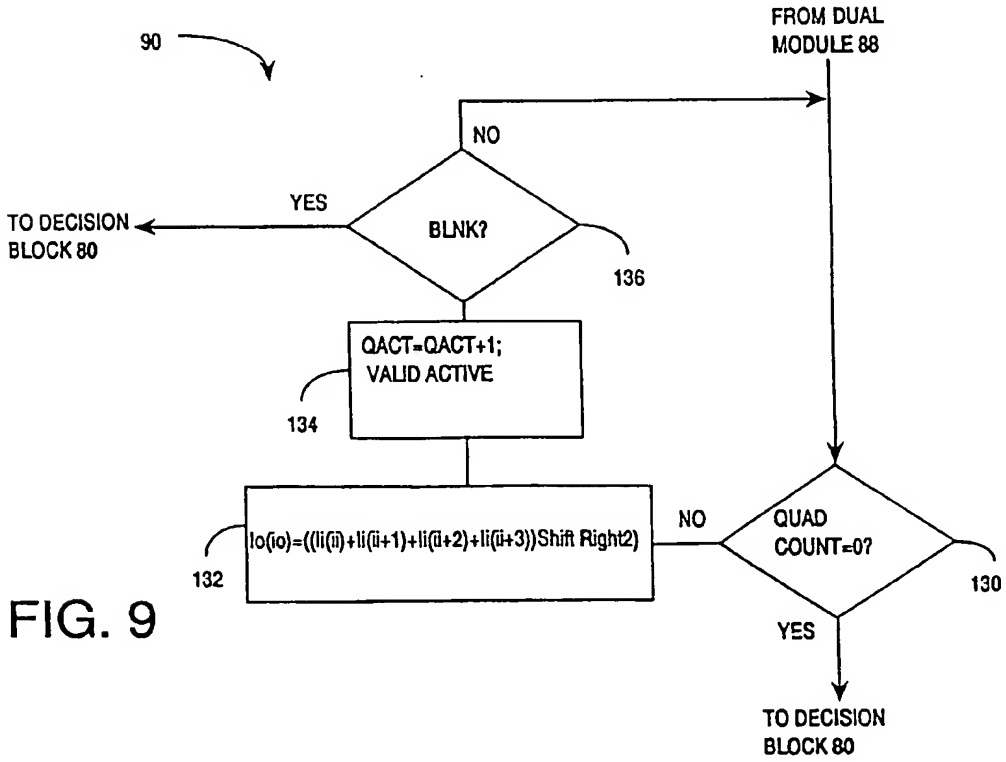
90
FROM DUAL MODULE 88
NO
YES
BLNK?
136
TO DECISION BLOCK 80
QACT=QACT+1; VALID ACTIVE
134
Io(io)=((Ii(ii)+Ii(ii+1)+Ii(ii+2)+Ii(ii+3))Shift Right2)
132
NO
QUAD COUNT=0?
130
YES
TO DECISION BLOCK 80

FIG. 9

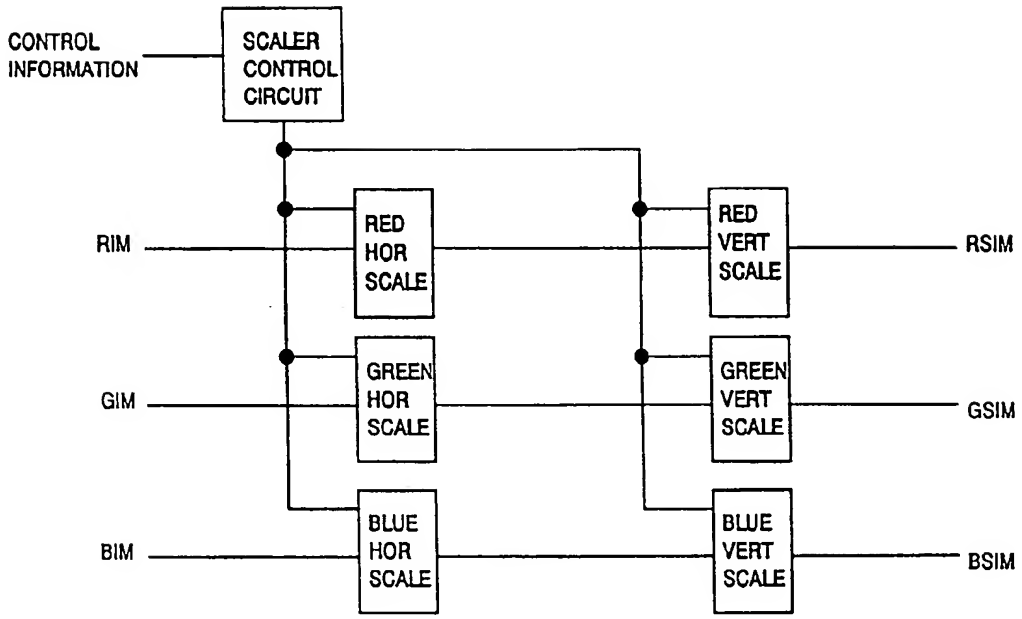
CONTROL INFORMATION
SCALER CONTROL CIRCUIT
RIM
GIM
BIM
RED HOR SCALE
GREEN HOR SCALE
BLUE HOR SCALE
RED VERT SCALE
GREEN VERT SCALE
BLUE VERT SCALE
RSIM
GSIM
BSIM

FIG. 10

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 30 0535

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	PATENT ABSTRACTS OF JAPAN vol. 6, no. 238 (E-144)26 November 1982 & JP-A-57 136 859 (NIPPON DENKI) 24 August 1982 * abstract *	1,2	H04N1/393 G06F15/62 G09G1/16
X	GB-A-2 157 126 (AMPEX) * abstract; figure 1 * * page 1, line 27 - line 57 * * page 2, line 23 - line 45 *	1,2	
X	EP-A-0 259 138 (CANON) * column 2, line 11 - column 3, line 27; figure 2 *	1	
A	EP-A-0 248 235 (NEC) * abstract; figures 1,2 * * page 3, line 26 - page 5, line 1 *	1	
A	EP-A-0 023 816 (XEROX) * abstract; figure 1 * * page 2, line 29 - page 5, line 17 *	1,3	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H04N
G06F
G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	23 APRIL 1992	SAAM C.

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